line emanating from the internal address generator 122. Applicant again submits a revised version of Figure 1 for the Examiner's consideration. Approval of this drawing change is hereby requested.

§103 Rejections

Claims 1-8 and 10-15 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Evoy et al. (U.S. Pat. No. 6,085,307) in view of McCarthy (U.S. Pat. No. 6,321,310). For the reasons outlined below, this ground of rejection is respectfully traversed.

The present application discloses a dual processor system 100 which includes a main processor 110 and a co-processor 120. The co-processor 120 includes a control register 121, an internal address generator 122, a data register 123 and memory 125. The internal address generator 122 utilizes a control word supplied by the main processor 110 on data bus 144 to 'generate' memory locations within the memory 125 in which incoming data will be stored.

The generation of memory locations by the internal address generator 122 permits multiple data words to be stored in memory 125 quickly and efficiently, as it eliminates the need for the main processor 110 to specify the memory location of each data word (See page 1, lines 22-26 and page 5, 27-31).

Evoy teaches a master-slave processor system 10 which includes a master processor 40 and a slave processor 50. The master processor 40 controls the operational state of the slave processor by programming internal control registers 56 of the slave processor 50. The system 10 also includes a system memory 25 which is shared by both the master and slave processors 40, 50.

As stated in Applicant's previous response, neither Evoy nor McCarthy disclose or suggest an "internal memory" (internal to the "second processor"), a "data register" or a "internal address generator" as specified in independent claims 1 and 10. Furthermore, Evoy fails to disclose or suggest any component which 'generates' or 'selects' memory locations for storage of incoming data as specified in independent claims 1 and 10.

In an effort to maintain the previous § 103 rejections without alteration, the Examiner now argues, inter alia, that:

(a) "...it would have been obvious to have each processor include its own internal memory...";

(b) it is well known to couple data (control) registers to a processor's internal memory; and

(c) it is well known to couple an internal address generator to a processor's internal memory and to a control register.

In response to the Applicant's arguments, the Examiner has proffered extensive explanations for why each of the above assertions is true, but has failed to point to "some teaching, suggestion or motivation in the prior art to make the specific changes made by the applicant" as required by the case law interpreting 35 U.S.C. § 103.

As previously noted by the Applicant, to establish a prima facie case of obviousness, there must be some teaching, suggestion or motivation in the prior art to make the specific change made by the applicant. In re Dance, 160 F.3d 1339, 1343 (Fed. Cir. 1998). Obviousness should be measured "at the time the invention was made" (i.e. the filing date of the application), and with no prior knowledge of the applicant's disclosure. In re Dembiczak, 175 F.3d 994, 998-999 (Fed. Cir. 1999).

In the present case, there is no teaching or suggestion in either Evoy or McCarthy which would lead one of ordinary skill in the art to create the system recited in claim 1 of the present application. As stated above, neither Evoy nor McCarthy discloses or suggests an "internal memory", a "data register", and an "internal address generator" which 'generates' address locations of a memory in which data is stored.

Additionally, obviousness cannot be established by hindsight combination to produce the claimed invention. In re Dance, 160 F.3d. at 1343. The Examiner must show reasons why the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the prior art references for combination in the manner claimed. In re Rouffet, 149 F.3d 1350, 1357 (Fed. Cir. 1998).

On several occasions throughout the Office Action, the Examiner points to the teachings of the present invention as a basis for maintaining an obviousness rejection. For example, at page 15 of the Office Action, the Examiner states:

> It has been explained by Applicant...that the purpose of Applicant's internal address generator is to utilize a control word supplied by the main processor in order to generate memory locations in which incoming data will be stored...It follows that this type of component would inherently exist within Evoy's system. [emphasis added].

The Examiner is clearly using the teachings of the present invention as a basis for maintaining an obviousness rejection (what is often referred to as "hindsight combination"), as prohibited by the above-cited cases. For the reasons discussed in the Applicant's previous response and highlighted above, reconsideration and withdrawal of this ground of rejection with respect to claims 1-8 and 10-15 is respectfully requested.

Furthermore, at several places throughout the § 103 rejection of claims 1-8 and 10-15 and the Examiner's associated arguments, the Examiner argues that certain elements missing from Evoy and McCarthy are "inherent" in the respective references. Inherency and obviousness are distinct concepts and should not be confused with one another. See, Kloster Speedsteel AB v. Crucible, Inc., 793 F.2d 1565 (Fed. Cir. 1986) and W.L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540 (Fed. Cir. 1983) [attached hereto].

Put simply, for teachings which the Examiner could not find in either Evoy or McCarthy, and which the Examiner could not allege were obvious teachings, the Examiner has stated that such teachings are "inherent" in the references. The following are examples:

(a) "it would be inherent that an internal address generator would be coupled..." (Page 4, Lines 7-10);

(b) "It is inherent that the instructions..." (Page 5, Lines 3-5); and

(c) "It follows that this type of component would inherently exist within in Evoy's system." (Page 15, Lines 4-5)

As discussed in Kloster, since inherency and obviousness are distinct concepts, when attempting to establish inherency in a § 103 obviousness rejection, one must show that the inherent teaching would have been obvious to one of ordinary skill in the art. Kloster, 793 F.2d at 1576 (Fed. Cir. 1986). The Examiner has failed to prove such a case here. It is submitted that the Examiner has improperly utilized the concept of inherency to 'cover up' teachings which are

neither disclosed nor suggested in Evoy and McCarthy. Accordingly, for at least this additional reason, reconsideration and withdrawal of this ground of rejection with respect to claims 1-8 and 10-15 is respectfully requested.

Claims 9 and 16 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Evoy in view of McCarthy, and further in view of Curran et al. (U.S. Pat. No. 6,334,179). For the reasons outlined below, this ground of rejection is respectfully traversed.

As discussed above, neither Evoy not McCarthy discloses or suggests an "internal memory", a "data register", and an "internal address generator" which 'generates' address locations of a memory in which data is stored. Curran also fails to disclose or suggest such structure.

Curran teaches a digital signal processor system 1 which includes a host Random Access Memory (RAM) and shared RAM banks 6, 7. Curran does not teach or suggest an "internal memory", a "data register", and an "internal address generator" which 'generates' address locations of a memory in which data is stored as required by independent claims 1 and 10. Therefore, reconsideration and withdrawal of this ground of rejection with respect to dependent claims 9 and 16 is respectfully requested.

In view of the foregoing remarks and amendments, Applicants submit that this application is in condition for allowance at an early date, which action is earnestly solicited.

The Assistant Commissioner for Patents is hereby authorized to charge any additional fees or credit any excess payment which may be associated with this communication to deposit account **04-1679**.

Respectfully submitted,

Dated: 2·13·03

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Version With Markings to Show Changes Made

Claims

1. (Unchanged) A dual processor system, comprising:

(a) a first processor coupled to a system address bus and a data bus; and

(b) a second processor coupled to the system address bus and to the data bus, the second processor comprising a control register having a control register system address, an internal memory, a data register having a data register system address and coupled to the internal memory, and an internal address generator coupled to the control register and to the internal memory, wherein:

a control word is written into the control register when the first processor places a control word having a burst mode bit and a starting internal address on the data bus and asserts the control register system address on the system address bus; and

the second processor enters a burst mode in which the internal address generator selects consecutive memory locations of the internal memory, starting at the starting internal address specified in the control word stored in the control register, during subsequent data transfer cycles, when the control word has a burst mode bit indicating burst mode.

2. (Unchanged) The dual processor system of claim 1, wherein the system is implemented as an integrated circuit.

3. (Unchanged) The dual processor system of claim 1 wherein the second processor remains in the burst mode only so long as the first processor asserts the data register system address on the system address bus.

4. (Unchanged) The dual processor system of claim 1, wherein, in a write burst mode, the first processor asserts the data register system address on the system address bus and writes subsequent data words on the data bus, and the internal address generator selects consecutive

memory locations of the internal memory, starting at the starting internal address, whereby the subsequent data words are written into the consecutive memory locations.

5. (Unchanged) The dual processor system of claim 1, wherein, in a read burst mode, the first processor asserts the data register system address on the system address bus and reads subsequent data words on the data bus, the internal address generator selects consecutive memory locations of the internal memory, starting at the starting internal address, and the data register reads data words at the consecutive memory locations and places said data words on the data bus, whereby the subsequent data words are read from the consecutive memory locations by the first processor.

6. (Unchanged) The dual processor system of claim 1, wherein the second processor is a co-processor.

7. (Unchanged) The dual processor system of claim 1, wherein:

the control word is written into the control register when the first processor places a control word having a burst mode bit and a starting internal address on the data bus and asserts the control register system address on the system address bus; and

the second processor enters a single data transfer mode in which the internal address generator selects the starting internal address specified in the control word stored in the control register, during a next data transfer cycle when the control word has a burst mode bit that does not indicate burst mode.

8. (Unchanged) The dual processor system of claim 1, wherein the first processor and second processor are intercoupled by the system address bus, the data bus, a chip select line, a read signal line, and a write signal line.

9. (Unchanged) The dual processor system of claim 1, wherein:

the internal memory comprises a plurality of memory blocks;

the control word comprises the burst mode bit field, a memory bank field which specifies a selected memory bank of the plurality of memory banks, and an internal bank address field which specifies the starting internal bank address within the selected memory bank; and

the internal address generator determines the starting internal address from the selected memory bank and the internal bank address of the control word.

10. (Unchanged) An integrated circuit having a second processor for transferring data with a first processor coupled to the second processor via a system address bus and a data bus, the second processor comprising a control register having a control register system address, an internal memory, a data register having a data register system address and coupled to the internal memory, and an internal address generator coupled to the control register and to the internal memory, wherein:

a control word is written into the control register when the first processor places a control word having a burst mode bit and a starting internal address on the data bus and asserts the control register system address on the system address bus; and

the second processor enters a burst mode in which the internal address generator selects consecutive memory locations of the internal memory, starting at the starting internal address specified in the control word stored in the control register, during subsequent data transfer cycles, when the control word has a burst mode bit indicating burst mode.

11. (Unchanged) The integrated circuit of claim 10, wherein the second processor remains in the burst mode only so long as the first processor asserts the data register system address on the system address bus.

12. (Unchanged) The integrated circuit of claim 10, wherein, in a write burst mode, the first processor asserts the data register system address on the system address bus and writes subsequent data words on the data bus, and the internal address generator selects consecutive

memory locations of the internal memory, starting at the starting internal address, whereby the subsequent data words are written into the consecutive memory locations.

13. (Unchanged) The integrated circuit of claim 10, wherein, in a read burst mode, the first processor asserts the data register system address on the system address bus and reads subsequent data words on the data bus, the internal address generator selects consecutive memory locations of the internal memory, starting at the starting internal address, and the data register reads data words at the consecutive memory locations and places said data words on the data bus, whereby the subsequent data words are read from the consecutive memory locations by the first processor.

14. (Unchanged) The integrated circuit of claim 10, wherein the second processor is a co-processor.

15. (Unchanged) The integrated circuit of claim 10, wherein the first processor and second processor are intercoupled by the system address bus, the data bus, a chip select line, a read signal line, and a write signal line.

16. (Unchanged) The integrated circuit of claim 10, wherein:

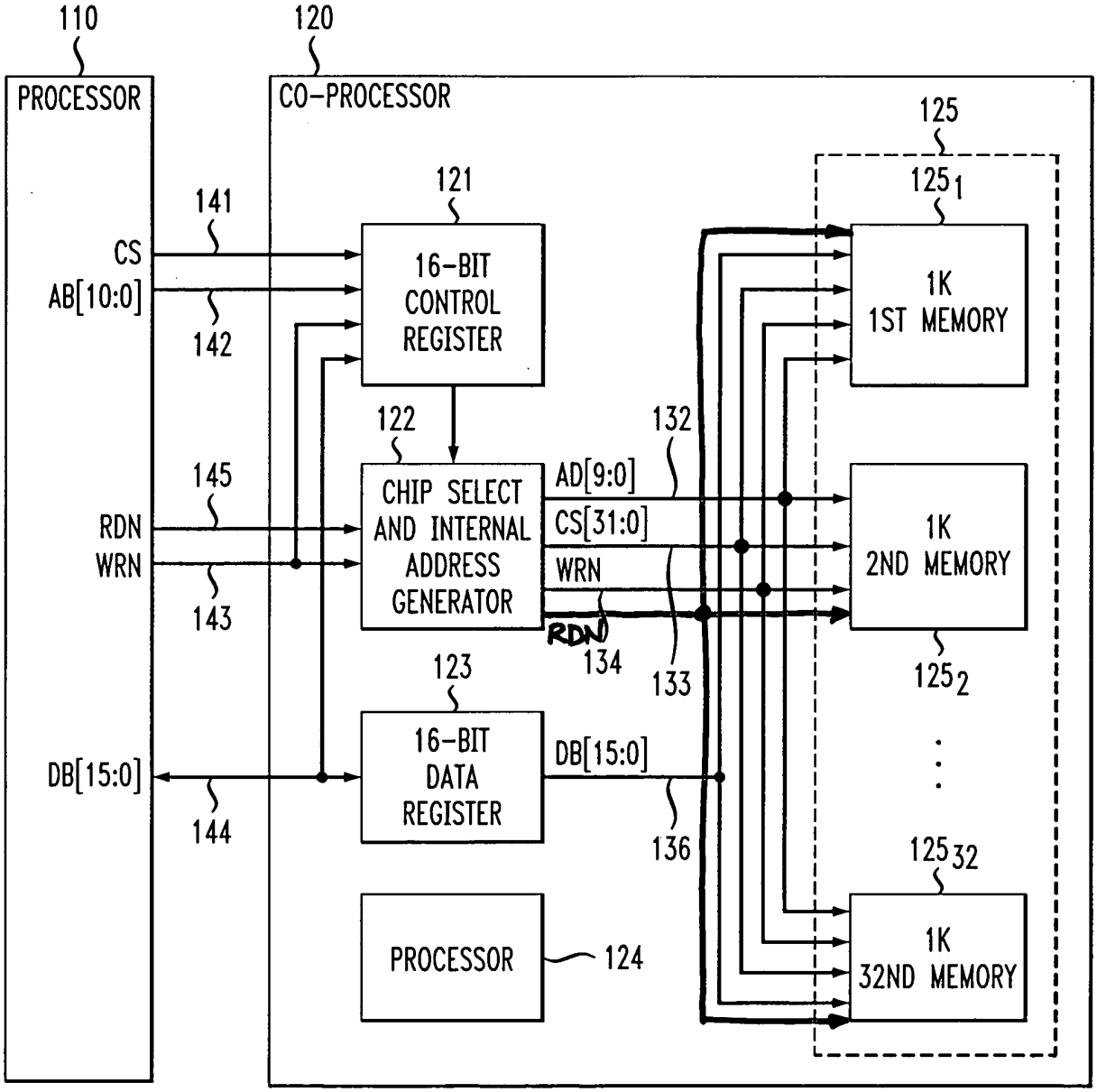
the internal memory comprises a plurality of memory blocks;

the control word comprises the burst mode bit field, a memory bank field which specifies a selected memory bank of the plurality of memory banks, and an internal bank address field which specifies the starting internal bank address within the selected memory bank; and

the internal address generator determines the starting internal address from the selected memory bank and the internal bank address of the control word.

FIG. 1

100



Docket No. D8143-00206; Inventors: El-Kik et al.
"Processor System Including Internal Address Generator for Implementing Single and bBrst Data Transfers"
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